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Stylesheet Version v1.1.1

Description

SEMICONDUCTOR PROCESS AND YIELD ANALYSIS INTEGRATED REAL-TIME MANAGEMENT METHOD

BACKGROUND OF INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to a management method, and more particularly, to an integrated real-time management method which provides semiconductor process and yield analysis for a plurality of management classes.

[0003] 2. Description of the Prior Art

[0004] A lot of data are used in the semiconductor process to monitor, control and improve all kinds of manufacturing processes. Please refer to Fig.1;Fig.1 is a block diagram of a semiconductor process 10 according to the prior art. The semiconductor process 10 processes a plurality of wafers 12 through seven steps, including a step of thin film 14, a step of diffusion 16, a step of photo 18, a step

of etch 20, a sample test 22, a wafer test 24, and a final test 26. A plurality of inspecting results are generated in each step to control and improve the semiconductor process 10. However, the inspecting results are merely raw data. In the prior art, there are no effective ways to integrate these raw data generated in each steps, therefore it is difficult to monitor the performance of the semiconductor process 10. . For different management classes, it is also hard to select the effective data from the large amount of the raw data.

SUMMARY OF INVENTION

[0005] It is therefore a primary objective of the claimed invention to provide a semiconductor process and yield analysis integrated real-time management method, to solve the above-mentioned problem.

[0006] According to the claimed invention, a semiconductor process and yield analysis integrated real-time management method comprises inspecting a plurality of semiconductor products with a plurality of items to generate and record a plurality of inspecting results during semiconductor process, classifying the semiconductor products as a plurality of groups with a default rule to generate and record an initial data in a database, indexing a plurality of semicon-

ductor product groups and the corresponding initial data from the database by a default product rule and parameter to calculate a corresponding analysis result, and displaying the analysis result according to the indexed semiconductor product groups and the initial data.

[0007] It is an advantage of the claimed invention that the semiconductor process and yield analysis integrated real-time management method can transfer the inspecting results of semiconductor process to all kinds of tables and charts for providing management and analysis. The tables and charts are integrated to present on the web page according to the management classes, which provides real-time interactive monitor and management.

[0008] These and other objectives of the claimed invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

BRIEF DESCRIPTION OF DRAWINGS

[0009] Fig.1 is a block diagram of semiconductor process according to the prior art.

[0010] Fig.2 is a diagram of semiconductor process and yield analysis management method according to the present

invention.

[0011] Fig.3 is a diagram of a displaying frame in the displaying step of Fig.2.

[0012] Fig.4 is a diagram of a displaying frame of the sample test class, the wafer test class, or the final test class shown in Fig.3.

[0013] Fig.5 is a diagram of a displaying frame of the DC maps and statistic charts shown in Fig.4.

[0014] Fig.6 is a diagram of a displaying frame of the defect inspection class shown in Fig.3.

[0015] Fig.7 is a diagram of a displaying frame of the Cp/Cpk statistics class shown in Fig.3.

[0016] Fig.8 is a diagram of a displaying frame of the alarming RT-SPC class shown in Fig.3.

[0017] Fig.9 is a diagram of a displaying frame of the RCA class shown in Fig.3.

[0018] Fig.10 is a diagram of a multiple-class management architecture.

DETAILED DESCRIPTION

[0019] Please refer to Fig.2. Fig.2 is a diagram of semiconductor process and yield analysis management method according to the present invention. The method includes the following steps:

[0020] step 30: inspecting a plurality of semiconductor products with a plurality of items during semiconductor process, and recording a plurality of inspecting results of each semiconductor product;

[0021] step 32: classifying the semiconductor products as a plurality of groups with a default rule, generating raw data according to the inspecting results of each group;

[0022] step 34: recording the raw data and the corresponding groups in a database;

[0023] step 36: indexing a plurality of semiconductor product groups from the database by a default product rule, indexing the corresponding raw data of each semiconductor product group by default parameters, and calculating a corresponding analysis result from the indexed semiconductor product groups and raw data with analysis modules; and

[0024] step 38: displaying the analysis result on a web page according to the indexed semiconductor product groups and the analysis results.

[0025] Please refer to Fig.3. Fig.3 is a diagram of a displaying frame 40 in the displaying step of Fig.2. The displaying frame 40 presents the analysis results 56 inspected in the semiconductor process shown in Fig.1 according to seven

classes, including a sample test class 42, a wafer test class 44, a final test class 46, a class of the Cp/Cpk statistics 50, an alarming real-time spec (RT-SPC) class 52, and a root case analysis (RCA) class 54. The analysis results of each class are described in the following.

[0026] Please refer to Fig.4. Fig.4 is a diagram of a displaying frame 60 of the sample test class 42, the wafer test class 44, or the final test class 46 shown in Fig.3. The displaying frame 60 includes a plurality of query items 62, a query button 64, a plurality of analytic items 66, and a plurality of analysis results 68. Users set the query items 62, including semiconductor products, manufacturing steps, and manufacturing date. As the query button 64 is pushed, the analysis results 68 are listed according to a plurality of lot numbers 65 and the analytic items 66, including the process lots, suffix of product names, test time, wafer numbers, yield, DC map of each wafer, statistic charts, repair rates, and so on. That is, the semiconductor products are grouped by wafer, lot, time (like test time or manufacturing date), and all related statistical analysis result (like yield, repair rate) can be accessed by users through an integrated interface as shown in Fig. 4. Wherein a plurality of DC map buttons 67 and a plurality

of statistic chart items 69 are hyper-linked to another display frame, which the shows DC map and statistic chart of each wafer in the assigned lot. Please refer to Fig.5. Fig.5 is a diagram of a displaying frame of the DC maps and statistic charts shown in Fig.4. According to query items 62 and the lot number 65, the DC map 71 and statistic chart 73 of each wafer are shown in the displaying frame 60 as an overview of the semiconductor processing in the assigned lot.

[0027] Please refer to Fig.6. Fig.6 is a diagram of a displaying frame 70 of the defect inspection class 48 shown in Fig.3. The displaying frame 70 includes a plurality of query items 72, a query button 74, an analysis result of bright field 76, and an analysis result of dark field 78. Users set the query items 72, including semiconductor products and manufacturing date. As the query button 74 is pushed on, the analysis result of bright field 76 and the analysis result of dark field 78 are listed according to the layer numbers of the wafers, which is similar to the analysis results 68 shown in Fig.4, including the process lots, suffix of product names, test time, wafer numbers, yield, DC map of each wafer, statistic charts, repair rates, and so on. That is, semiconductor products could be grouped ac-

cording to processes types (like dark field and bright field), and the corresponding analysis results can be accessed through an interface like shown in Fig. 6.

[0028] Please refer to Fig.7. Fig.7 is a diagram of the displaying frame 80 of the Cp/Cpk statistics class shown in Fig.3. The displaying frame 80 presents statistic data of four segments of semiconductor process, including a segment of diffusion 82, a segment of etch 84, a segment of photo 86, and a segment of thin film 88. The statistic data of each segment are shown in a statistic chart 90 and a statistic table 92. The statistic chart 90 shows the trend of statistic values versus time. The statistic table 92 shows the statistic values, including the average, the standard deviation, Cp, and Cpk of each manufacturing step.

[0029] Please refer to Fig.8. Fig.8 is a diagram of a displaying frame 100 of the alarming RT-SPC class shown in Fig.3. The displaying frame 100 includes an alarming table 102, which shows the alarming condition of each segment of semiconductor process by manufacturing date. The details of each segment are shown in an alarm list 104, which shows the manufacturing lots, the manufacturing equipments, the manufacturing date, and the cause of out-spec according to the lot numbers of the wafers. In addition,

users can interactively comment in the alarm list 104.Fig.9 is a diagram of a displaying frame 110 of the RCA class shown in Fig.3. The displaying frame 110 includes a plurality of analysis items112, ananalysis button 114, and a plurality of analysis results 116. Users set the analysis items 112, including manufacturing technology, manufacturing product groups, manufacturing products and manufacturing layers. As the analysis button 114 is pushed on, the analysis results 116 are listed by manufacturing variable names, including manufacturing time, the average, the standard deviation, and so on.

[0030] Please refer to Fig.10. Fig.10 is a diagram of a multiple-class management architecture 120. The multiple-class management architecture 120 includes a director 122, a plurality of department managers 124, a plurality of section managers 126, and a plurality of engineers 128. The statistic data are present for each class of managers through a lot of analytic modules, including T-test, a one-way analysis of variance (ANOVA), a two-way analysis of variance, or box plots. The analytic results are also present according to the different management classes. For example, the director 122 monitors the yield value for yield improvement, the department managers 124 moni-

tor the inspecting results of defect inspection to deal with the problems of the processing layers, the section managers 126 monitor the statistic results of each processing section, and the engineering 128 monitor the inspecting results of each test to in-line control processing quality. That is, the presentation of the statistical analysis results can be fully customized by users of different management classes. In practical, the invention can provide a plurality of default displaying modes, each mode recording a predetermined way of displaying analysis results. Then a user can set a costumed displaying mode by selecting among the default displaying modes. For example, an engineer user may prefer to obtain in-line QC information through the invention, then the engineer user can select related default displaying modes to show in-line QC analysis result. On the other hand, a department manager may prefer to monitor long-term yield performance of a given kind of product or a given process, so the manager can select related default displaying modes to show corresponding analysis results.

[0031] In contrast to the prior art, the present invention semiconductor process and yield analysis integrated real-time management method can transfer the inspecting results

of semiconductor process to all kinds of tables and charts for providing management and analysis. The tables and charts are integrated to present on the web page according to the management classes, which provides real-time interactive monitor and management.

[0032] Those skilled in the art will readily observe that numerous modifications and alterations of the device may be made while retaining the teachings of the invention. Accordingly, that above disclosure should be construed as limited only by the metes and bounds of the appended claims.